THROUGH SILICON VIAS AND THERMOCOMPRESSION BONDING USING INKJET-PRINTED GOLD NANOPARTICLES FOR HETEROGENEOUS MEMS INTEGRATION

N. Quack^{1,2}, J. Sadie², V. Subramanian², and M. C. Wu^{1,2}* ¹Berkeley Sensor and Actuator Center, University of California, Berkeley, USA ²Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, USA

ABSTRACT

We present a novel technique for heterogeneous integration using gold filled Through Silicon Vias (TSV) and thermocompression bond bumps formed in a single fabrication step, using gold nanoparticles dispensed by inkjet printing. Gold-filled TSV arrays (12 x 12, via radius 50µm, pitch 250µm) have been demonstrated using this method. Void free, filled TSVs are reported, and thermocompression bonding yielded seamless interfaces. Die shear tests show good bond strength, and sub- Ω via resistances were measured. The presented integration process exhibits a low temperature budget (≤250°C), allows good alignment, and is compatible with substrates of different sizes and materials, enabling the heterogeneous integration of known-good-dies (KGD) which may have been fabricated in different technologies.

KEYWORDS

Through Silicon Via (TSV), 3D Integration, Nanoparticle, Inkjet-Printing, MEMS, Flip-Chip Bonding, Chip Scale Packaging (CSP), Known-Good-Die (KGD).

INTRODUCTION

Heterogeneous integration of multiple functional platforms (which might differ in size and materials) into a single chip, such as MEMS and photonics with CMOS electronics, has immediate impact on applications such as integrated chip scale 3D imaging systems [1], high performance focal plane array image sensors [2], or optical phased array for fast beamforming [3]. In order to realize these applications, die-level chip stacking and interconnection techniques that utilize conductive vertical vias are particularly attractive solutions (see Fig. 1).

Many approaches have been demonstrated for waferscale via formation using Deep Reactive Ion Etching (DRIE) or laser drilling, and trench filling with copper electroplating [4], tungsten metal fill [5], or island insulation of doped silicon pillars in the handle wafer in a via-first on silicon-on-insulator (SOI) process [6]. While these techniques are effective on large scales, they are not suitable for rapid prototyping of heterogeneously integrated modules that involves different substrates and often at die level rather than whole wafers. In addition, approaches to adapt current 3D heterogeneous integration schemes to such Known-Good-Die (KGD) integration require substantial processing [7]. Thus, an alternative technique for via filling that optimizes flexibility and performance, and furthermore reduces cost would be an invaluable addition to research and development heterogeneous integration process flows. Recently, multiproject-wafer (MPW) runs have become available in silicon photonics [8], which have spurred increased

interest in 3D integration processes compatible with small dies, typically in the range of a few mm².



Figure 1: Heterogeneous integration of CMOS, Silicon Photonics and III-V active MEMS photonics in a single chip [1].

Nanoparticle inks have recently been demonstrated as suitable candidates for inkjet-printed microelectronic circuits, using low processing temperatures and showing outstanding electrical performance of the sintered material [9]. Inkjet printing of TSVs by covering via side walls with silver particles has been demonstrated recently [10]. Our previous work has demonstrated the ability to print high-aspect ratio features appropriate for wafer level bonding as well as TSV interconnect applications [11]. However, direct bonding of inkjet-printed TSV dies has not been demonstrated. In this paper, we demonstrate the first completely filled TSV fabricated by inkjet printing including thermocompression bonding using gold TSV filling and solder bump deposition by inkjet printing in a single process step.

HETEROGENEOUS INTEGRATION Inkjet Printing Procedure

The schematic inkjet printing setup is shown in Fig. 2. Commercially available Harima NPG-J gold nanoparticle ink is printed with a MicroFab MJ-AT $60\mu m$ diameter nozzle on a custom built inkjet printer.



Figure 2: Inkjet printing setup at UC Berkeley [12].

The sample is placed on a computer controlled motorized micrometer precision stage. Temperature is adjusted to typically 140°C during printing, and alignment is achieved using a digital microscope. During inkjet printing on the heated substrate, the solvent containing the gold nanoparticles evaporates, and the gold nanoparticles coalesce. A final sintering step after printing at 250°C for 5 to 60 minutes melts the gold nanoparticles to form a dense, seamless material. The melting occurs at a greatly decreased temperature due to thermodepression [9, 11] Details on the printer setup and the printing process have been reported elsewhere [12].

TSV Filling

The schematic process flow for filling TSV by inkjet printing is shown in Fig. 3. Trenches with via depth of 100 μ m were fabricated using DRIE on a 6" SOI wafer (100 μ m device layer, 2 μ m buried oxide, 500 μ m handle layer). The buried oxide serves as effective etch stop.



Figure 3: Schematic cross section representation of the ink-jet printed TSV sample preparation.

By adjusting the number of droplets, the TSV can be completely filled (Fig. 4). Typically, 35 droplets are sufficient to fill a 100 μ m TSV completely. Circular TSVs with radii from 25 μ m to 50 μ m, and square TSVs with sides from 50 μ m to 100 μ m were successfully filled. Our achievable via size is currently limited by the printer nozzle size and can be scaled using smaller nozzle sizes.



Figure 4: SEM top view images of single a) square ($80\mu m$ square length) and b) circular $r=40\mu m$ via filled with gold by inkjet printing (after sintering). The number of printed droplets was adjusted to completely fill the circular via.

Bond Bump Deposition and Array Printing

Increasing the total number of droplets above the necessary amount to fill a trench results in pillar growth out of the TSV. We have investigated the mechanisms of pillar growth on flat surfaces in detail previously [12]. The growth rate and hereby the pillar radius can be adjusted by the stage temperature during printing and the height of the pillars can be adjusted from a few to several hundred microns by varying the total amount of droplets. Figs. 5a and 5b show two printed linear arrays, for which

the total number of droplets was adjusted to fill the square vias completely. For the circular vias, the excess amount of volume is transformed into pillars during growth. Fig. 5c demonstrates the capability to homogeneously print large arrays of TSV (here 12 x 12 array of TSV with a radius of $r=40\mu$ m, and pitch $p=250\mu$ m), demonstrating the potential for high density TSV array fabrication.



Figure 5: SEM micrographs of a) a linear array of 3 squares (80µm square length), b) 3 circular vias (40µm radius) and c) large arrays (partial view of 12x12 array).

Thermocompression Bonding

In order to investigate the fill quality of the TSV, a SEM cross section analysis was performed, using the process flow shown in Fig. 6. Vias with a depth of 100μ m were etched by DRIE on a 6" Silicon Wafer, which was subsequently diced. Inkjet printing was performed on a heated stage at 140° C. Die alignment and thermocompression bonding was performed using a Finetech Fineplacer Lamda flip chip bonder. The thermocompression bonding recipe consisted in a 250°C sintering step for 10min with 1N applied force (4mm x 4mm sample).



Figure 6: Schematic process sequence for TSV cross section visualization: a) wafer level DRIE of deep trenches, dicing; b) die level TSV filling and c) bond bump deposition in the same inkjet printing step. d) Die level alignment and bonding, including metal sintering and e) underfill for mechanical stabilization during cross section dicing process.

During this simultaneous bonding and sintering step, the coalesced nanoparticles melt and form a seamless bond interface. For cross section visualization, the bonded dies were diced at the center of the TSV. Cyanoacrylate based adhesive was used as efficient underfill for stabilization of the bonded dies during cross section dicing. Fig. 7 shows a cross section view of a successfully bonded pair.



Figure 7: Cross section images of two bonded dies: b) SEM overview image and a) close up optical micrograph showing the 6 circular vias in the center, and c) the TSV etch pattern top view. The cross sections show good filling and repeatability of the process. Via radii are $40\mu m$.

The cross section images of diced TSVs reveal *void free filling* of the circular vias (Fig. 8a). Using the identical ink volume in square vias results in sidewall covering only (Fig 8b). Bond gaps were typically below $2\mu m$, and post-bonding alignment accuracy better than $6\mu m$.



Figure 8: Cross-section images of diced Through Silicon Vias. The images reveal complete filling of the a) circular vias, while the (b) square vias are only covering the surface.

ELECTRICAL INTERCONNECT AND DIE SHEAR STRENGTH Sample Preparation

Both die shear strength measurements and electrical interconnect measurements were performed. Fig. 9 shows the schematic sample preparation, which consisted in 100µm DRIE on a SOI wafer, electrical insulation by a low temperature oxide (LTO) deposition (134nm), TSV inkjet printing and bond bump deposition. Bond substrates for these tests consisted oxidized silicon dies with a patterned Cr/Au coating (2nm/50nm). The flip-chip bonded samples (step 4 in Fig. 9) were used for bond

strength measurements. For the electrical interconnect measurement samples, the backside is removed by an isotropic SF₆ dry etch, and the oxide opened by a HF wet etch. Subsequent metal deposition and patterning allow for daisy-chain interconnection (step 7 in Fig. 9).



Figure 9: Sample preparation for bond strength and electrical interconnect measurements.

Die Shear Strength

Measurements of die shear strength were performed using a standard shear strength measurement procedure on a Nordson Dage Bond Tester 4000. The die shear strength were performed on 4mm x 4mm TSV samples bonded to 8mm x 8mm substrate dies as described above. Fig. 10 shows the die shear strength measurement schematically (*inset*), and a typical measurement result of a die shear strength measurement for 12 x 12 array. The measurement shows yields a shear strength of 1.9kg, which confirms good bond strength.



Figure 10: Die shear strength measurement setup (inset) and typical die shear strength measurement, showing failure at 1.9kg applied shear force.

Electrical Interconnects

Resistance of the TSV was measured using four point probe measurement, as schematically depicted in Fig. 11. In the particular sample, metal sidewall coverage was limited, so that the TSV were probed directly as shown in Fig. 11c. Total measured resistance for two interconnects as shown in Fig. 11b, were measured at typically $800m\Omega$. This resistance is largely dominated by the metal interconnect pad on the bond substrate. Assuming bulk resistivity for the thin film resistivity on the bond substrate, the extracted TSV resistance amounts to typically $50m\Omega$. This corresponds to less than 10% the bulk resistivity of gold and allows for improvement of the inkjet printing conditions for further reduction in TSV resistance.



Figure 11: Electrical interconnect measurement procedure: (a) sample before backside removal, (b) schematic cross section view of a measurement of a single pair of bonded TSVs, and (c) top view microscope view.

DISCUSSION AND CONCLUSIONS

We have reported experimental results on gold-filled TSVs and gold solder bumps for heterogeneous integration applications. The gold in TSVs have been deposited by inkjet printing in a single, low-temperature fabrication step. TSV with radii from 25μ m to 50μ m have been successfully filled, and cross-section SEM analysis shows void-free filling of the TSVs. The demonstrated via radii of 25μ m allow high density vertical interconnects, though the density can further be increased: our achievable via size is currently limited by the printer nozzle size (diameter 60μ m) and can readily be scaled using smaller nozzle sizes.

The fabricated dies have been successfully bonded by gold thermocompression bonding at 250°C. Die shear strength measurements confirm good bond strength, and sub- Ω via resistances were measured.

This first demonstration of inkjet-printed filled gold TSVs shows the potential of this technology for die level heterogeneous integration of various technology platforms, such as CMOS electronics, MEMS and Silicon Photonics.

ACKNOWLEDGEMENTS

This project is partially supported by Ultratech Inc. and the Defense Advanced Research Projects Agency (DARPA) E-PHI program under Grant No. HR0011-11-2-0021. The TSV printing substrates and bond substrates were fabricated in the Marvell Nanofabrication Laboratory at the University of California, Berkeley.

REFERENCES

- N. Quack, J. Ferrara, S. Gambini, S. Han, C. Keraly, P. Qiao, Y. Rao, P. Sandborn, L. Zhu, S.-L. Chuang, E. Yablonovitch, B. Boser, C. Chang-Hasnain, M. C. Wu, "Development of an FMCW LADAR Source Chip using MEMS-Electronic-Photonic Heterogeneous Integration", GOMACTech Conference, 13-4, Las Vegas, NV, USA, March 12-14, 2013.
- [2] M. Motoyoshi, "Through-Silicon Via (TSV)", Proc. of IEEE, Special Issue on 3-D Integration Technologies, Vol. 97, No. 1, 2009, pp. 43-48.
- [3] B.W. Yoo, M. Megens, T. Chan, T. Sun, W. Yang, C.J. Chang-Hasnain, D.A. Horsley, and M.C. Wu, "Optical phased array using high contrast gratings for 2D beamforming and beamsteering," Optics Express, April 2013 (accepted, in press).
- [4] U. Kang, H.-J. Chung, S. Heo, D.-H. Park, H. Lee, J.-H. Kim, S.-H. Ahn, S.-H. Cha, J. Ahn, D.-M. Kwon, J.-W. Lee, H.-S. Joo, W.-S. Kim, D.-H. Jang, N.-S. Kim, J.-H. Choi, T.-G. Chung, J.-H. Yoo, J. S. Choi, C. Kim, Y.-H. Jun, "8 Gb 3-D DDR3 DRAM Using Through-Silicon-Via Technology", IEEE Journal of Solid-State Circuits, Vol. 45, No. 1, 2010, pp. 111-119.
- [5] J. Burns, B. Aull, C. Chen, C.-L. Chen, C. Keast, J. Knecht, V. Suntharalingam, K. Warner, P. Wyatt, D.-R. Yost, "A Wafer-Scale 3-D Circuit Integration Technology", IEEE Transactions on Electron Devices, Vol. 53, No. 10, 2006, pp. 2507-2516
- [6] M. Rimskog, T. Bauer, "High density through silicon via (TSV)", 2008 Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS, Nice, France, 9-11 April 2008.
- [7] Y. Temiz, M. Zervas, C. Guiducci, and Y. Leblebici, "Die-Level TSV Fabrication Platform for CMOS-MEMS Integration", in Digest Tech. Papers Transducers'11 Conference, Beijing, China, June 5-9, 2011, pp. 1799-1802.
- [8] K. Bourzac, "Photonic chips made easier," Nature, vol. 483, no. 7390, p. 388, 2012.
- [9] T. Bakhishev and V. Subramanian, "Investigation of Gold Nanoparticle Inks for Low-Temperature Lead-Free Packaging Technology", J. Elec. Mat., Vol. 28, No. 12, pp. 2720-2725, 2009.
- [10] A. Rathjen, Y. Bergmann, K. Krüger, "Feasibility Study: Inkjet Filling of Through Silicon Vias (TSV)", in NIP28: International Conference on Digital Printing Technologies and Digital Fabrication 2011, Quebec, Canada, Sept. 2012, pp. 456-460.
- [11] P. Buffat and J.P. Borel, "Size Effect on the Melting Temperature of Gold Particles", Phys. Rev. A, Vol. 13, No. 6, pp. 2287-2298, 1975.
- [12] J. Sadie, S. Volkman, V. Subramanian, "Demonstration of Inkjet Printed Nanoparticle-based Inks for Solder Bump Replacement", in Proc. of 2012 45th International Symposium on Microelectronics, San Diego, CA, USA, Sept. 2012, pp. 419-424.

CONTACT

*N. Quack, tel: +1-805-4558412; niels@quack.ch